Myricom DBL–
Integrated FPGA Firmware and Software

Enabling extreme low-latency and advanced trading capabilities

CSPi's Myricom® DBL technology powers the ARC Series of network adapters, driving down system-level Tick-To-Trade latency and enabling advanced financial trading capabilities. It is a tightly-integrated combination of FPGA firmware and software libraries.

System-level Tick-To-Trade Latency

DBL drives down Tick-To-Trade latency at multiple points in the trading process, allowing your application to deliver higher fill rates.

First, it minimizes **Receive Latency** by exploiting the parallel processing capabilities of powerful FPGAs to direct subsets of a multi-cast market feed to specified CPU cores, totally bypassing the OS kernel.

At initialization, your application uses our DBL software library for a quick and easy set-up of the selectors, targeting data from a specific address and port to an assigned ring. See Figure 1
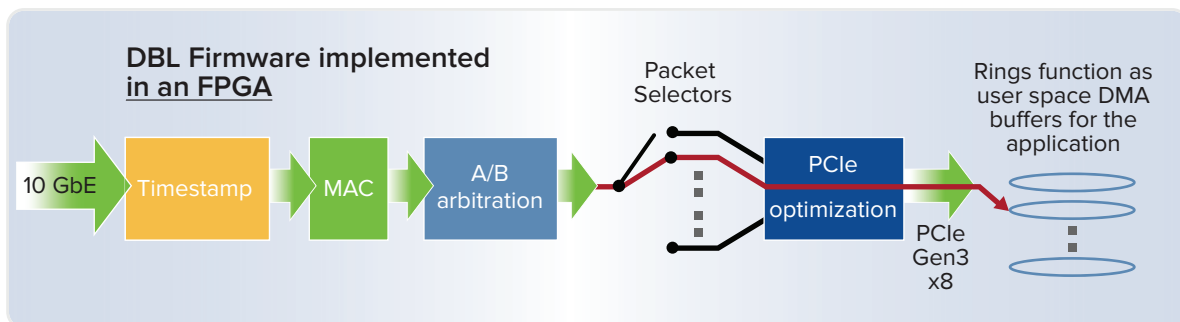

Figure 1 – DBL Firmware Moves Data to an Assigned Ring

Every packet does not need to move into the user space data rings, just the packets your application uses.

Integrated DBL Software Accelerates the Application Layer

You can compress total Tick-To-Trade latency even further by accelerating your application with the tightly integrated DBL software. Acceleration is delivered by Kernel Bypass Stacks, which move UDP packets directly to your application in user space. Doing that eliminates the cost of CPU context switches and also enables deployment of special-purpose network stacks in user space, which are faster than the general purpose stacks inside the kernel. The DBL software provides 3 interface options for implanting a faster network stack:

- **Transparent Sockets** allow your application to accelerate stack performance without code changes. Standard socket calls access the low latency DBL stack without recompiling.

- The **DBL API** accesses a set of Myricom-optimized sockets. It requires a software recompile, with renamed socket calls, but delivers even lower latency.

- **Raw Mode** allows customers to implement their own custom stacks with the Myricom ARC network adapters, using either raw sockets or a proprietary API.

In general, Raw Mode is useful for customers who have created their own UDP networking stacks to work with another vendor's products and are now migrating to the Myricom network adapters. Most longtime Myricom customers use the DBL API, gaining the advantages of a latency-optimized UDP stack function without investing time or money in additional software development.
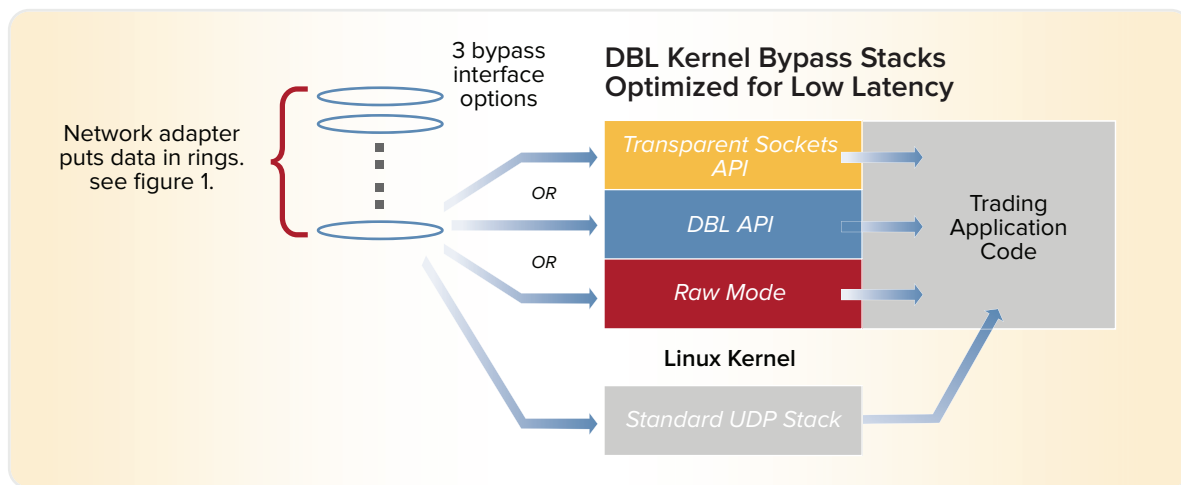

Figure 2 – Kernel Bypass Stacks Optimized for Low Latency

Reducing Send Latency

DBL software accelerates outbound order processing by pre-populating the TCP/IP stack in user space, then filling in just the variable information from the application before sending the BUY/SELL order packet to the adapter. The Send Latency is further minimized with extremely efficient PCIe to Ethernet conversion firmware. Each new generation of FPGAs represents faster silicon, making the firmware faster and moving Send (and Receive) Latency closer to zero.

Hardware Acceleration for Applications That Use A/B Arbitration

If your application uses A/B feed arbitration you can offload that function to the ARC network adapter hardware, gaining a reduction in software overhead and removing significant traffic from your server's shared DRAM subsystems, a common location for performance bottlenecks. The adapter's specialized DBL firmware can arbitrate the A and B sides of multiple feeds for both fiber and microwave sources, effectively implementing 4-way arbitration.

The A/B arbitration is invisible to the trading application, as the adapter provides an A feed that contains the first packets to arrive from either the real-world A or B side. Your application can query the adapter for a count of lost packets recovered or for real time information on individual feed status. Turning on hardware-based A/B arbitration adds zero latency to the adapter's receive path.

Precise Hardware Timestamps

With DBL firmware, ARC network adapters are able to track latency in real-time with less effort and more accuracy than expensive packet capture devices, using precise hardware timestamps on both ingress and egress packets. This unique capability allows your application to calculate latency without needing to tag TCP/IP orders with UDP sequence numbers, for simplified trading performance verification. It also prepares systems for compliance with the detailed reporting required by the 2018 MIFID II regulations.
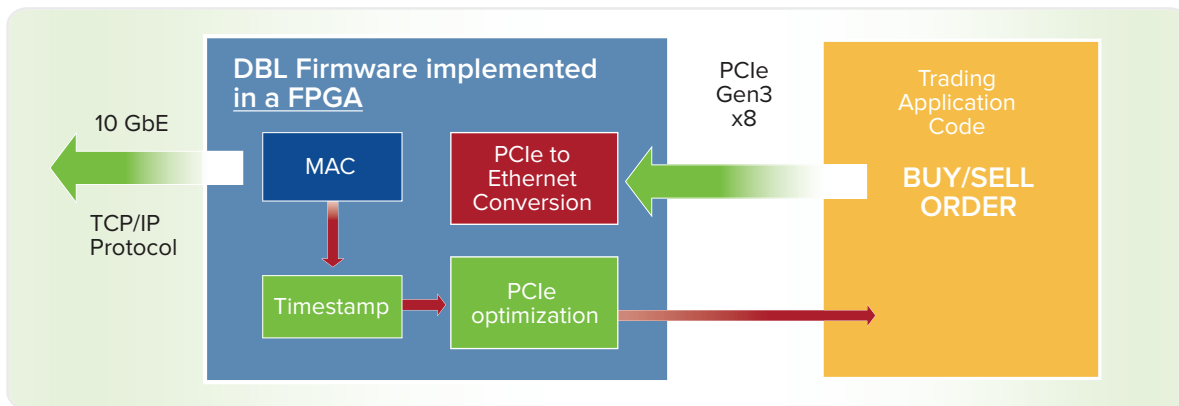

Figure 3 – Transmit Timestamping

An Architecture for Future Enhancements

DBL's firmware and software architecture is designed to support a steady stream of enhancements, so CSPi can continue to rapidly respond to market requirements by delivering new functionality on existing network adapters. The architecture also supports timely upgrades to new network adapter models employing the most recent FPGA technology, with current DBL functionality moving quickly to new silicon without lengthy and complex ASIC design cycles.

Summary

DBL technology powers the Myricom ARC Series of network adapters, the industry's lowest-latency, fully -featured market feed connections for financial trading. DBL firmware drives Receive + Send hardware latency close to zero while the tight integration between the firmware and DBL software is optimized with functions to accelerate your trading application. Moving forward, the FPGA-based architecture is designed for continual enhancements and periodic upgrades to new silicon.
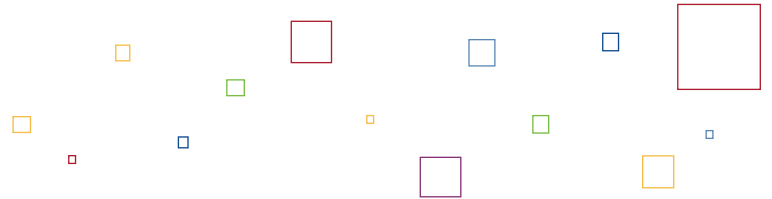
About CSPi

CSPi (NASDAQ: CSPi) is a global technology innovator driven by a long history of business ingenuity and technical expertise. A market leader since 1968, we are committed to helping our customers meet the demanding performance, availability, and security requirements of their complex network, applications and services that drive success.

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